Lecture 5: Materials and technologies
Silicon photonic process integration

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After more than a decade of exploratory research, silicon photonics has now become a business segment coveted by various industrials. The rationale behind the emergence of silicon photonics is to take advantage of the production capacities of CMOS foundries, that is, big volume and low cost manufacturability. The semiconductor industry benefits from a long experience in silicon processing take advantage of process maturity of this non-zero impulse to launch silicon photonics and ensure a quick qualification of technology nodes with respect to targeted photonic device performances. We learn from recent publications that most of the processes associated to the current silicon photonic production can be imported with minimum implementation from CMOS fab processes. Nevertheless, a few exceptions still exist to fulfill completely the needs of a totally integrated photonic circuit.
In this lecture, we will review the motivations for photonic integration using silicon technology and more precisely cmos fabrication capabilities. Typical silicon photonic fabrication flow will be detailed, highlighting the specific needs versus cmos process. The major particularities of silicon photonics are mainly related to the silicon patterning. For example, in silicon photonics the integrated devices are optically interconnected at silicon level. Thus, silicon patterning must be done at one step to guarantee the auto-alignment of structures. Another issue is the sidewall waveguide roughness which directly impacts the optical performances of the devices. A specificity of silicon photonic technology is the use of pure germanium epitaxy as an absorbing material for photo detection function. Figure 2 presents a tilted SEM pictures of an integrated Butt-coupled lateral Germanium photodiode. Doped silicon junctions required also some specific controls and integration strategies to address the needs of active photonic device, mainly modulator. Process robustness and impact on variability on silicon photonics device will be also discussed in this lecture.

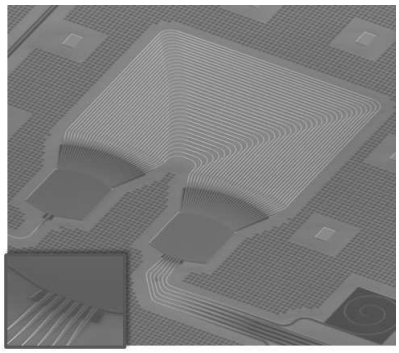

Fig.1: Array Wave Guide

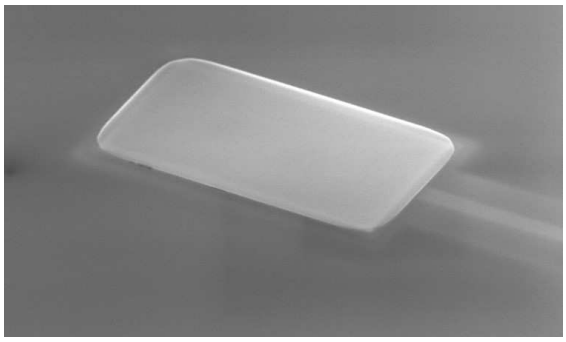

Fig.2: Integrated Butt-coupled lateral Germanium photodiode