Photonic Packaging at a glance

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Packaging of photonic and electronic devices in very high density multifunctional optoelectronics modules is becoming of strategic importance for the next generation of optical components at lower costs and compatible with high-volume manufacturing. In order to penetrate the markets, a packaging design flow must be developed leading to a process standardization. First of all, some design rules are needed to ensure the users to implement their own chip-level designs that can be more easily packaged and ultimately drives down the costs. The packaging design flow follows a three-levels macro-design areas: .the optical design the electrical design and the mechanical design. From a practical point of view, due to the presence of thermal gradients and thermal cross-talks induced by on-chip lasers and other active optical elements, heaters and electronic components, the behavior of the photonic chip may be altered and performances of the overall system compromised. Further, thermal gradients induce also mechanical stresses that can be a critical issue for example thinking of fiber coupling. It is therefore mandatory to develop tools able to study and manage these issues in a multi-physical environment.

Fiber-to-waveguide coupling still present the major technological challenges. Two distinct approaches for fiber- optical chip coupling are considered and discussed: edge-coupling and grating-coupling. Edge-coupling exploits lensed fibers either spot size converters (SSCs) and can offer lower insertion-losses and broadband coupling, but has significantly more stringent alignment tolerances especially when fiber array are needed. The use of an optical interposer is considered as custom solution to improve coupling efficiency and pitch matching between the fiber and the IN/OUT waveguides arrays. Grating-coupling in addition to offering relaxed-alignment tolerances, allow for optical access at any point on the PIC surface and remove the need for PIC polishing or surface preparation.

The packaging of electrical interconnects on a photonics chip can be just as challenging as the optical packaging, especially for high-speed electrical signals (even greater than 40 GHz). Electrical packaging of PICs with electronic drivers, amplifiers and other control circuitry is becoming an ever greater challenge, as demand grows for higher levels of photonic-electronic integration. Common approaches are hybrid integration, either flip-chip bonding of an electronic-IC onto the PIC, or simply connecting the PIC directly to a PCB. Furthermore, the integration of electronic-ICs with PICs introduces additional complications to the thermal management of the module.

A thermal cross-talk and circuital analysis is presented for a novel, flexible MUX/DEMUX based on micro-ring filters on a SOI platform, enabling spectrally efficient aggregation/segmentation of different super-channels. A thermal-stress multi-physical simulation is also discussed for a complex photonic package, taking into account issues such as temperature stabilization and dissipation, fiber coupling misalignment due to thermo-mechanical stresses and the impact of thermal and stress gradients on the optical parameters of the photonic chip.

References

[1] Pavarelli, Nicola, Jun Su Lee, and Peter A. O'Brien. "Packaging challenges for integrated silicon photonic circuits." *SPIE Photonics Europe*. International Society for Optics and Photonics, 2014.

[2] F. Della Corte et al., "Temperature dependence of the thermo-optic coefficient of InP, GaAs, and SiC from room temperature to 600 K at the wavelength of 1.5μm", Applied Physics Letters 77.11, 2000.

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